JPEG-Codec-IP-Core (Decoder) for FPGAs

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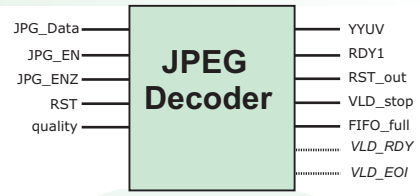
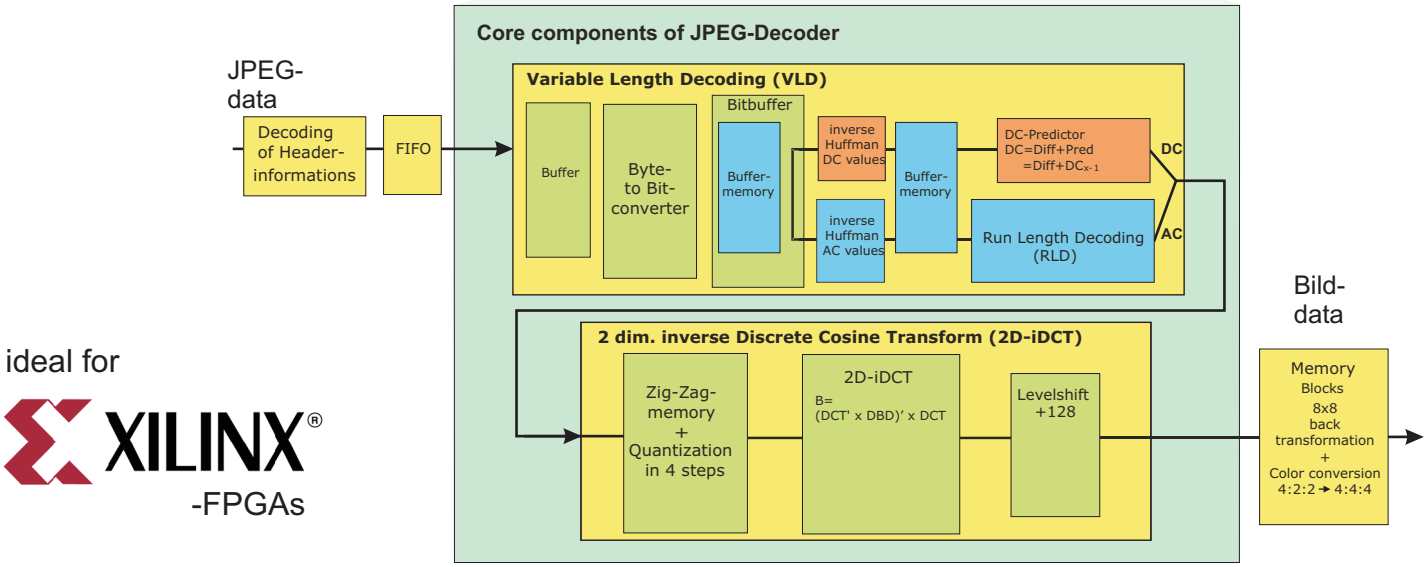
Applications

- Digital photo- or video decoding
- Surveillance systems
- Videoconferencing systems
- low-latency automotive or real-time systems





ideal for XILINX® -FPGAs

- JPEG-compression/Decompression according to „baseline process“ by CCITT T.81 (ISO/IEC 10918-1).
- JPEG codec consists of a separate encoder and decoder section, which can be operated individually or in parallel. High performance and robustness has been proven in practical applications.
- Slightest delay between the data input and the compressed data output (6...15 µs).
- The high-performance codec is suitable for high-quality single images, and/or Motion JPEG (MJPEG).
- Minimum space consumption at high speed in XILINX FPGAs (Spartan-6 < 1060 Slices).
- Quality and compression can be selected with 4 or more predefined or customized quantization tables. Data amount of the compressed image rages between 1% and 33% of the amount of data of the uncompressed image.
- Complete reset before and after each image, i.e.each frame has the same initial conditions in the Motion JPEG. Therefore different video streams are decoded serially in one core.
- Easy insertion into an existing HDL program or connect with program modules through defined interfaces.
- Programming of the whole JPEG codec was designed with a graphical user interface (Matlab/Simulink with XILINX System Generator) as a modular structure.
- Images can have any size (e.g. 64 k x 64 k).
- Optional modules for video camera control, Bayer-Pattern-Interpolation,color space conversion, RAM access, etc. are available. Individual adaptation of IP-Cores are possible.
- Core for XILINX FPGAs applicable (Spartan-3-Family, Spartan-6, Virtex-4, Virtex-5, Virtex-6, 7th family Artix, Kintex, Virtex, ZYNQ).

Space requirements and speed

The **JPEG decoder** (core components 2D-iDCT and VLD) is listed as example in the following XILINX FPGAs with the space requirements according to Place & Route::

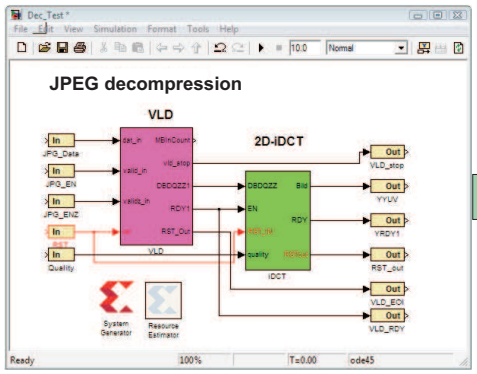
FPGA	Slice Reg	Slice LUTs	used slices	DSP48 or emb. Mult.	BlockRAM	BlockRAM /kbit
Spartan-3E	2138	4291	2519	1	4	64
Spartan-6	2117	2728	1056	1	3	48
Virtex-5	2124	3008	1075	1	2	72
Virtex-6	2115	2798	1019	1	2	72
Virtex-7	2048	2729	959	1	2	72
Kintex-7	2047	2734	1010	1	2	72

The maximum possible system frequencies of the cores and the processing speeds are listed below for FPGAs with the appropriate speed grade for the maximum system clock and maximum pixel clock for the encoder:

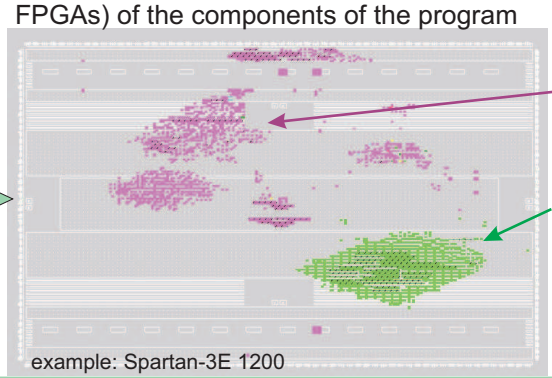
FPGA	Speedgrade	t_{max} /ns	$f_{System\ max}$ /MHz	$f_{Pixel\ max}$ /MHz (24 bit/Pixel)
Spartan-3E	4	9,09	110	55
Spartan-6	2	7,33	136	68
Spartan-6	3	5,95	168	84
Virtex-5	2	4,24	236	118
Virtex-6	2	4,16	240	120
Virtex-7	3	4,42	226	113
Kintex-7	2	4,27	234	117

For high and highest quality of the compressed images, the quantization and speed can be adjusted.
Our development team is also available for each adaptation and assistance with this and other IP cores.

Matlab/Simulink program



Floor plan (location of the elements within the FPGAs) of the components of the program



Options

- Header decoding and video presentation
- Image line memory internally/externally RAM with pixel ordering (YYUV) as postprocessing
- additional FIFOs for compressed image data and multi-camera connection
- Development services about FPGA functions and applications

ordering information

JPEG-Dec-HQ	JPEG decoder for single images of the highest quality
JPEG-Dec-Video	JPEG decoder for video streams
JPEG-Dec-NV	Postprocessing of the image data at decoder output

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