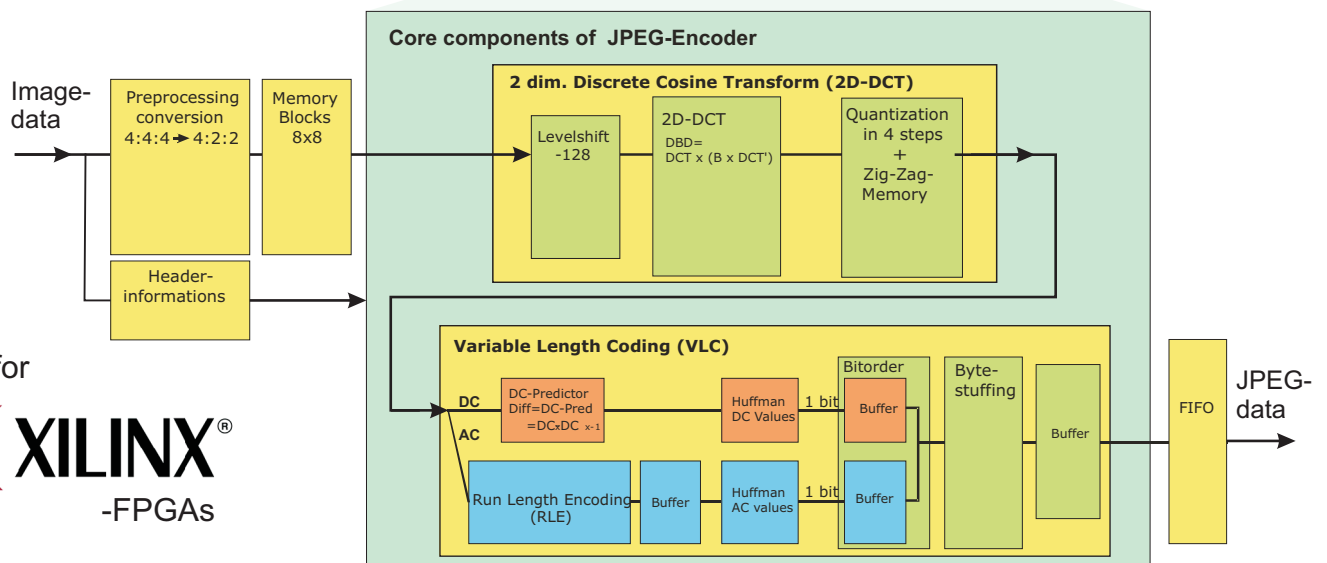
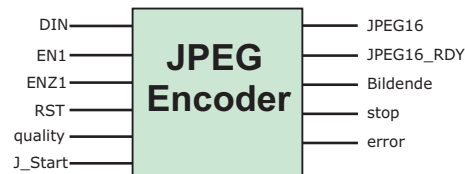


# JPEG-Codec-IP-Core (Encoder) for FPGAs

## Applications

- Digital cameras and -camcorders
- Surveillance systems and cameras
- Videoconferencing systems, smart cameras
- low-latency cameras (slightest delays)



ideal for



- JPEG-compression/Decompression according to „baseline process“ by CCITT T.81 (ISO/IEC 10918-1).
- JPEG codec consists of a separate encoder and decoder section, which can be operated individually or in parallel. High performance and robustness has been proven in practical applications.
- Slightest delay between the data input and the compressed data output (2...8 µs).
- The high-performance codec is suitable for high-quality single images, and/or Motion JPEG (MJPEG).
- Minimum space consumption at high speed in XILINX FPGAs (Spartan-6 < 1200 Slices).
- Quality and compression can be selected with 4 or more predefined or customized quantization tables. Data amount of the compressed image ranges between 1% and 33% of the amount of data of the uncompressed image.
- Complete reset before and after each image, i.e. each frame has the same initial conditions in the Motion JPEG.
- Easy insertion into an existing HDL program or connect with program modules through defined interfaces.
- Programming of the whole JPEG codec was designed with a graphical user interface (Matlab/Simulink with XILINX System Generator) as a modular structure.
- Images can have any size (e.g. 64 k x 64 k).
- Optional modules for video camera control, Bayer-Pattern-Interpolation, color space conversion, RAM access, etc. are available. Individual adaptation of IP-Cores are possible.
- Optional with automatic compression control for limited data rate (amount of data of compressed image is adapted effectively to the bandwidth of the interface).
- Core for XILINX FPGAs applicable (Spartan-3-Family, Spartan-6, Virtex-4, Virtex-5, Virtex-6, 7<sup>th</sup> family Artix, Kintex, Virtex, ZYNQ).

## Space requirements and speed

The **JPEG encoder** (core components 2D-DCT and VLC) is listed as example in the following XILINX FPGAs with its space requirements according to Place & Route:

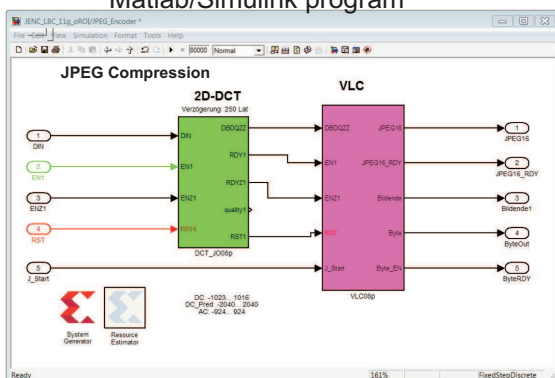
FPGA	Slice Reg	Slice LUTs	used Slices	DSP48 or emb. mult.	BlockRAM	BlockRAM /kbit
Spartan-3E	2234	3442	2769	1	5	80
Spartan-6	2240	2790	1192	1	3+2	56
Virtex-5	2199	2818	1173	1	1+3	80
Virtex-6	2205	2653	1098	1	1+3	80
Virtex-7	2201	2640	1142	1	1+3	80
Kintex-7	2184	2591	1080	1	1+3	80

The maximum possible system frequencies of the core and the processing speeds are listed below for FPGAs with the appropriate speed grade for the maximum system clock and maximum pixel clock for the encoder:

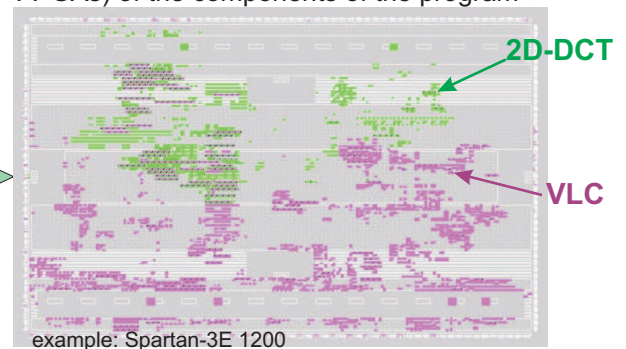
FPGA	Speedgrade	$t_{max}$ /ns	$f_{system\ max}$ /MHz	$f_{pixel\ max}$ /MHz (24 bit/pixel)
Spartan-3E	4	8,3	120	60
Spartan-6	2	5,68	176	88
Spartan-6	3	4,81	208	104
Virtex-5	2	4,17	240	120
Virtex-6	2	3,12	320	160
Virtex-7	2	3,29	304	152
Kintex-7	2	3,67	272	136

For high and highest quality of the compressed images, the quantization and speed can be adjusted. Our development team is also available for each adaptation and assistance with this and other IP cores.

Matlab/Simulink program



Floor plan (location of the elements within the FPGAs) of the components of the program



## Options

- Header generation and image preparation
- Image line memory internally/externally with pixel ordering (YYUV)
- additional FIFOs for compressed image data
- Development services about FPGA functions and applications

## ordering information

- JPEG-Enc-HQ** JPEG encoder for single images of the highest quality
- JPEG-Enc-Video** JPEG encoder for video streams
- JPEG-Enc-VV** Preprocessing of the image data to the encoder input

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